3-phase N+P Half-bridge Gate Drive Chip CH282

Datasheet

Version: V1.1

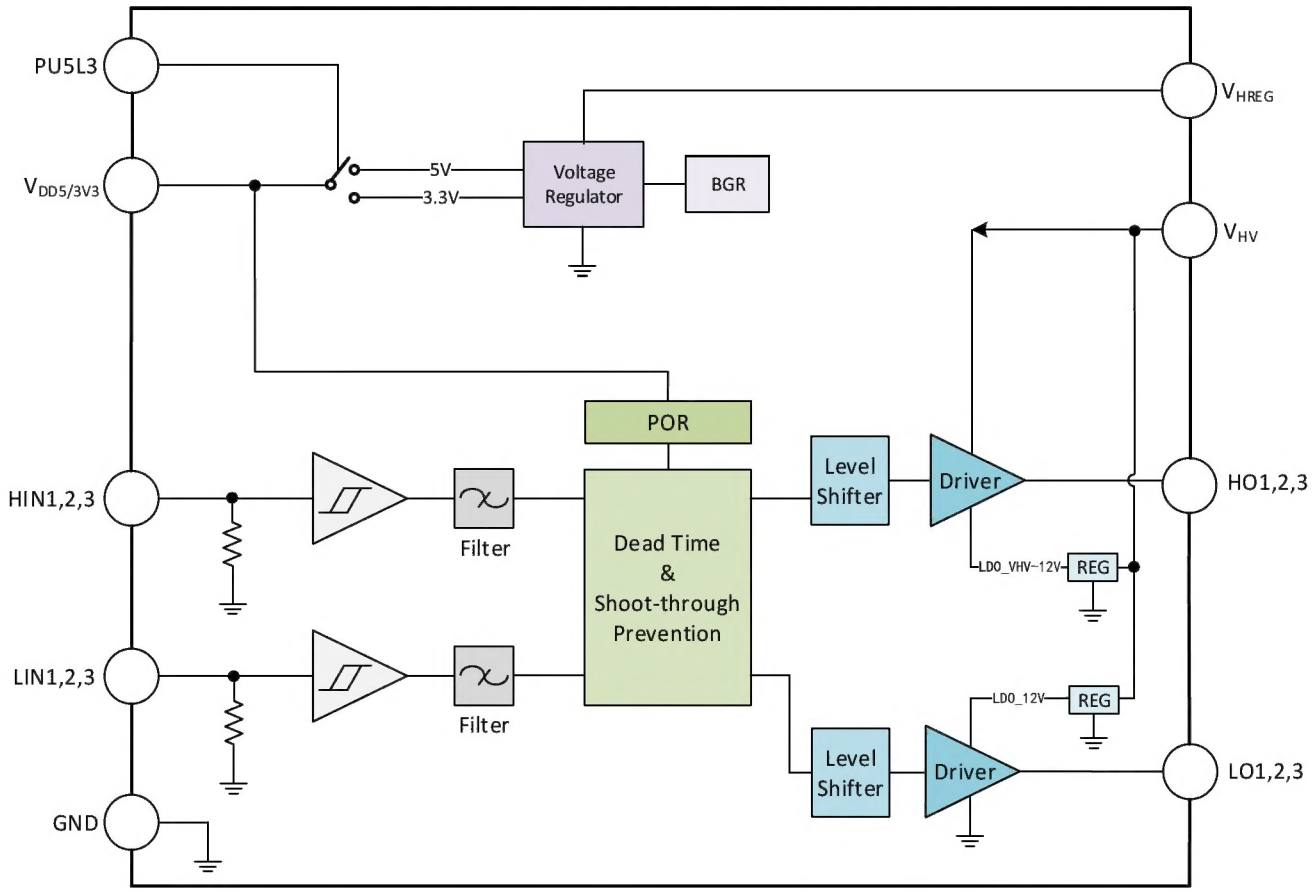
https://wch-ic.com

1. Overview

CH282 is an industrial-grade 3-phase half-bridge gate drive chip, mainly used for gate driving of 3 pairs of N-channel and P-channel MOSFET power tubes in 3-phase brushless DC motors below 24V.

The CH282 chip integrates 3 independent high-speed half-bridges and supports gate drive of 3 pairs of P/N type power tubes; it has a fully static low-power design and a built-in voltage regulator to provide power for MCU or other controllers; it has built-in PWM signal input circuit, dead-time control and high and low side MOSFET Shoot-Through Prevention circuit, undervoltage protection circuit, level shift circuit and output drive circuit.

The following figure shows the structural block diagram of CH282 for reference only.



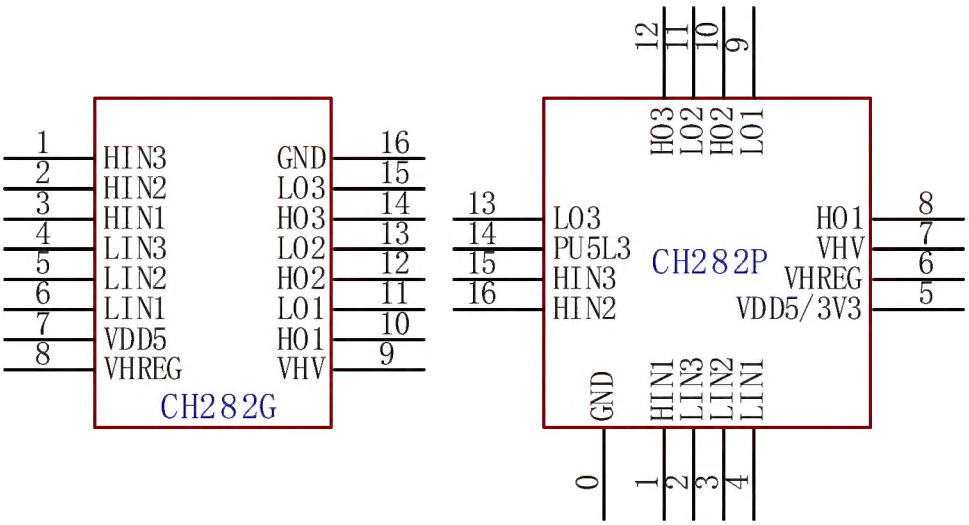
2. Features

- Integrated 3-channel independent half-bridge drivers, supporting 3 pairs of P+N MOSFET.
- Built-in voltage regulator can provide simple power supply for MCU and save external LDO regulator.
- A low-side driver positive power supply and a high-side driver negative power supply are internally

generated for limiting driving at high voltage.

- High closing current and low opening current realize fast closing and slow opening, and the opening current is as high as 120mA.
- MCU compatible with 5V or 3.3V power supply, supporting PWM signal in the range of 2.5V ~ 6V.
- Fully static low-power design, supporting PWM switching frequency from 0 to 500kHz.
- Built-in dead-time control prevents high-side and low-side MOSFET power tubes from passing through.
- Built-in undervoltage protection prevents MOSFET power tube from working at too low voltage.
- Provide package forms such as SOP16 and QFN16.

3. Pinouts



Package Form	Body Size	Pin Pitch		Package Description	Order Model
SOP16	3.9mm	1.27mm	50mil	Small Out-Line Package	CH282G
QFN16	3*3mm	0.5mm	19.7mil	Quad Flat No-Lead Package	CH282P

Note: Pin #0 refers to the EPAD of the QFN package.

4. Pin Definitions

Table 4-1 Pin definitions

Pin No.		Pin name	Type	Pin description
CH282G	CH282P			
9	7	VHV	P	CH282 drive power input, requires an external capacitor of at least 3.3uF, and 10uF is recommended.
16	0	GND	P	Common ground terminal, 0V reference point
6/5/4	4/3/2	LIN1/LIN2/LIN3	I	Logic input for low-side gate driver, built-in weak pull-down resistor, high level turn-on, LO is in phase with LIN
3/2/1	1/16/15	HIN1/HIN2/HIN3	I	Logic inverting input of high-side gate driver, built-in weak pull-down resistor, high level turn-on, HO is inverted with HIN
11/13/15	9/11/13	LO1/LO2/LO3	O	Low-side gate driver output, default low, active high.
10/12/14	8/10/12	HO1/HO2/HO3	O	High-side gate driver output, default high, active low
8	6	VHREG	P	The power input of the voltage regulator must be powered, usually through a resistor or directly connected to VHV
-	5	VDD5/3V3	P	Voltage regulator output, nominal 5V or 3.3V, is selected by PU5L3 and used as MCU power supply. At least 3.3uF capacitor needs to be externally connected, and 10uF is recommended.
7	-	VDD5	P	Voltage regulator output, rated at 5V, is also used as MCU power supply. At least 3.3uF capacitor needs to be externally connected, and 10uF is recommended
-	14	PU5L3	I	VDD5/3V3 pin output voltage selection, built-in weak pull-up current, floating or short-circuiting VDD5/3V3 to select 5V, connect GND and select 3.3V

5. Function Description

5.1 Gate Driver (LO1/2/3 and HO1/2/3)

CH282 integrates 3 independent half-bridge drivers. Each half-bridge driver consists of a low-side driver and a high-side driver, which drive the gate of the low-side N-type MOSFET power tube and the gate of the high-side P-type MOSFET power tube respectively.

The output pins LO1/2/3 of the low-side driver are in phase with their corresponding logic input pins LIN1/2/3 respectively. The LO pin output is valid when it is high level, and the default is low level, turning off the N-type power tube.

The output pins HO1/2/3 of the high-side driver are respectively inverted with their corresponding logic input pins HIN1/2/3. The HO pin output is valid at a low level and is high by default, turning off the P-type power tube.

The positive power supply of the low-side driver is stepped down from VHV in CH282 to generate LDO_12V, and the negative power supply is GND, which corresponds to LDO_12V and GND when driving high and driving low respectively.

The positive power supply of the high-side driver is VHV, and the negative power supply is reduced from VHV in CH282 to generate LDO_VHV-12V, which corresponds to VHV and LDO_VHV-12V when driving high and driving low respectively.

5.2 Logic Input (LIN1/2/3 and HIN1/2/3)

The logic input pin of CH282 has Schmidt input characteristics and is compatible with 5V or 3.3V logic levels. It is used to connect microcontrollers such as MCU and input PWM control signals. Turn off the MOSFET power tube when input low level, and turn on the MOSFET power tube when input high level.

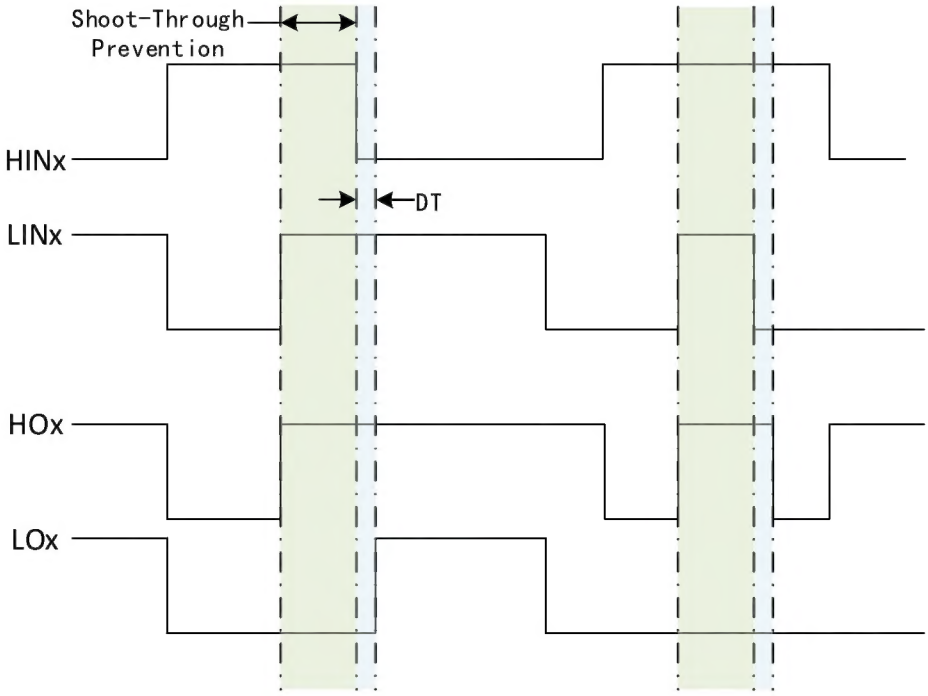
A weak pull-down resistor is built into the logic input pin, which ensures that the power tube is in the off state during virtual welding, MCU reset or input disconnection.

5.3 Shoot-Through Prevention

CH282 has a built-in protection circuit to prevent the high-side and low-side power tubes from conducting at the same time, which leads to the direct connection between power supply and ground.

As shown in the following figure, when the low-side logic input LIN and the high-side logic input HIN of the same phase input high levels at the same time, the internal straight-through prevention circuit will force the driver to output the default level (HO is high level and LO is low level) to turn off the power tube. When one of the input signals becomes low, the driver output needs a dead time delay to output an effective level. This protection mechanism avoids the simultaneous conduction of high and low power tubes caused by abnormal input, thus reducing the straight-through loss and protecting the power tubes.

Figure 5-1 Shoot-Through Prevention



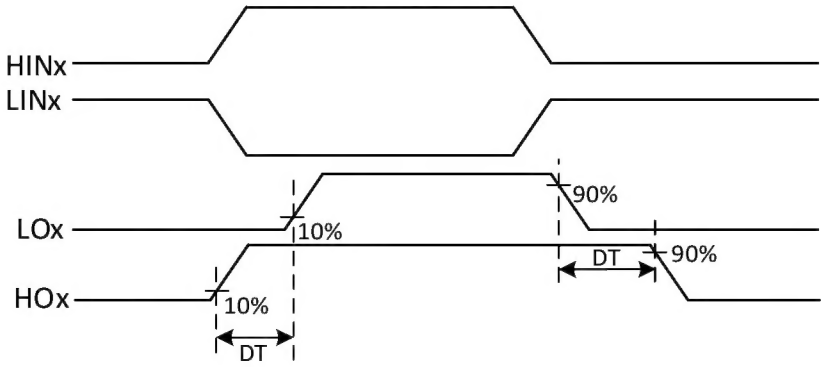
5.4 Dead Time

CH282 has built-in dead time protection circuit. During the dead time, the driver is forced to output the default level, that is, HO is high and LO is low. The dead time is used to turn on another power tube after one power tube is turned off, so as to prevent the high and low power tubes from going through at the same time.

Controllers such as MCU usually also support flexible dead time setting, and the final dead time is the larger value of MCU dead time and CH282 internal dead time. CH282 internal dead time is usually the minimum requirement in general application scenarios, and more flexible MCU dead time is usually considered in combination with MOSFET device characteristics, EMI requirements, power consumption and other factors.

The following figure describes the timing relationship among dead time, logic input signal and driver output signal.

Figure 5-2 Dead time



5.5 Voltage Regulator (VDD5/3V3)

The voltage regulator is used to generate the power supply for the core, and also serves as the power supply for microcontrollers such as MCU. The power input is the VHREG pin, the regulated output is the VDD5/3V3 pin,

and the PU5L3 pin is used to select the VDD5/3V3 pin to output 5V or 3.3V according to the MCU voltage.

When the driving power supply voltage VHV is not high, VHREG can directly supply power to VHV. When the voltage of VHV is high, in order to reduce the pressure difference and reduce the heat generation of CH282, it is optional to divide the series resistance of VHV according to the load current and then connect it to the pin of VHREG. It is suggested that the pressure difference between VHREG and VDD5/3V3 should be controlled at not less than 2V, and the greater the pressure difference, the more heat generated by CH282.

The VDD5/3V3 pin needs to be externally connected with at least 3.3uF capacitor, and 10uF is recommended. PU5L3 pin has built-in weak pull-up current. When it is suspended or shorted to VDD5/3V3, the regulator is selected to output 5V voltage, and when PU5L3 is shorted to GND, the regulator is selected to output 3.3V voltage.

The gate driver circuit requires the VHREG supply to provide a reference; if VHREG is powered down, then CH282 enters a reset state and the VHV supply draws essentially no current.

5.6 Drive Power VHV and Undervoltage Protection

VHV is the input of CH282 driving power supply, which generates power supplies LDO_12V and LDO_VHV-12V inside the chip. The VHV quiescent current is reduced significantly after the supply voltage falls below 12V.

The internal power supply LDO_12V is used as the positive power supply of the low-side driver to limit the gate-source voltage difference of the N-type MOSFET when the VHV voltage is high. LO corresponds to LDO_12V and GND when driving high and low levels respectively.

The internal power supply LDO_VHV-12V is used as the negative power supply of the high-side driver, which limits the gate-source voltage difference of the P-type MOSFET when the VHV voltage is high, and corresponds to VHV and LDO_VHV-12V when HO drives high level and low level respectively.

The VHV peak current is relatively large and requires an external capacitor of at least 3.3uF. 10uF or larger is recommended.

The built-in undervoltage protection circuit monitors the VHV voltage. When the VHV voltage is low, the driver is forced to output the default level (HO is high level, LO is low level) to turn off the power tube to avoid overheating caused by insufficient power tube opening. When VHV rises and exceeds the threshold voltage VHVUVR, CH282 releases the force and works normally; when VHV drops and is lower than the threshold voltage VHVUVF, CH282 forces the driver to output the default level and stops working.

6. Parameters

6.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Symbol	Parameter		Min.	Max.	Unit
T_A	Ambient temperature during operation		-40	105	℃
T_S	Ambient temperature during storage		-40	150	℃
T_J	Junction temperature range		-40	150	℃
V_{HV}	Drive power supply voltage		-0.4	28	V
V_{HREG}	Input supply voltage of the voltage regulator		-0.4	28	V
$V_{DD5/3V3}$	Voltage at the regulator output pin		-0.4	7	V
V_{IN}	Input voltage of logic signal LIN or HIN		-0.4	7	V
V_{HO}	Voltage at the high-side driver output pin HO		-0.4	V_{HV}+0.4	V
V_{LO}	Voltage at the low-side driver output pin LO		-0.4	V_{HV}+0.4	V
I_{AVVHV}	VHV pin continuous input current			50	mA
I_{AVGND}	GND pin continuous current			100	mA
V_{ESD}	HBM ESD tolerant voltage		2		KV
P_D	Maximum power consumption of the whole chip @TA≤25℃ (including the power consumption of drivers and regulators).	CH282G		700	mW
		CH282P		700	mW
θ_{JA}	Packaging thermal resistance	CH282G		110	℃/W
		CH282P		100	℃/W

Note: When testing pin current and driver short-circuit current, it is recommended to adopt low duty cycle pulse test and consider the timely heat dissipation of the chip.

6.2 General Operation Condition (Test conditions: T_A=25℃, typical value, V_{HV} = V_{HREG} = 15V)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{HV}	Power supply voltage		6	6~24	26	V
V_{LDO_12V}	Internal power supply LDO_12V no-load output voltage		11	12	14.5	V
$V_{LDO_VHV-12V}$	Internal power supply LDO_VHV-12V no-load output voltage		V_{HV}-14.5	V_{HV}-12	V_{HV}-11	V
V_{HREG}	Input power supply voltage of voltage regulator		6	7	26	V
$V_{DD5/3V3}$	Output voltage of voltage regulator	PU5L3 suspended	4.9	5	5.1	V
		PU5L3 to GND	3.23	3.3	3.37	V
$I_{VDD5/3V3}$	Regulator load current at VDD5/3V3 pin				30	mA
$V_{IN1/2/3}$	Input voltage of logic signal LIN or HIN		0		6	V

6.3 Electrical Parameters (T_A = 25℃, V_{HV} = V_{HREG} = 15V, V_{DD} = 5V, C_L = 1nF)

6.3.1 Power Current (Low-power test condition: VHIN1/2/3 = VLIN1/2/3 = 0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{QVHV}	Driver Power Supply V_{HV} Quiescent Current	$V_{HV} = V_{HREG} = 15V$	40	60	90	uA
		$V_{HV} = V_{HREG} = 11V$	0	7	15	uA
		$V_{HV} = 24V, V_{HREG} = 0V$		0		uA
I_{QREG}	Voltage regulator V_{HREG} quiescent current	PU5L3 suspended or connected to GND	30	45	70	uA
I_Q	V_{HV} and V_{HREG} combined quiescent current	$V_{HV} = V_{HREG} = 6V$		41		uA
		$V_{HV} = V_{HREG} = 11.5V$		52		uA
		$V_{HV} = V_{HREG} = 12.5V$		97		uA
		$V_{HV} = V_{HREG} = 24V$		130		uA

6.3.2 Logical Input

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	LIN/HIN high-level input threshold voltage		2.5		6	V
V_{IL}	LIN/HIN low-level input threshold voltage		0		0.8	V
V_{IS}	LIN/HIN input hysteresis voltage		0.3	0.5	0.8	V
R_{PD}	LIN/HIN built-in pull-down resistor		70	100	140	KΩ
I_{IN+}	LIN/HIN high-level input bias current	$V_{IN} = 5V$	35	50	72	uA
		$V_{IN} = 3.3V$	23	33	48	uA
I_{IN-}	LIN/HIN low-level input bias current	$V_{IN} = 0V$		0	2	uA
V_{IHV5}	PU5L3 high level input threshold voltage		2.0		6	V
V_{ILV5}	PU5L3 low level input threshold voltage		0		0.6	V
I_{PU}	PU5L3 built-in pull-up current	PU5L3 < 0.8V		1.5	140	uA
		PU5L3 > 1.3V		4	330	uA

6.3.3 Low-voltage Protection

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{HVUVR}	V_{HV} undervoltage protection start voltage		4.8	5.2	5.7	V
V_{HVUVF}	V_{HV} undervoltage protection shutdown voltage		4.4	4.9	5.3	V

V_{HVUVS}	V_{HV} undervoltage protection hysteresis voltage		0.1	0.3	0.6	V

6.3.4 Driver

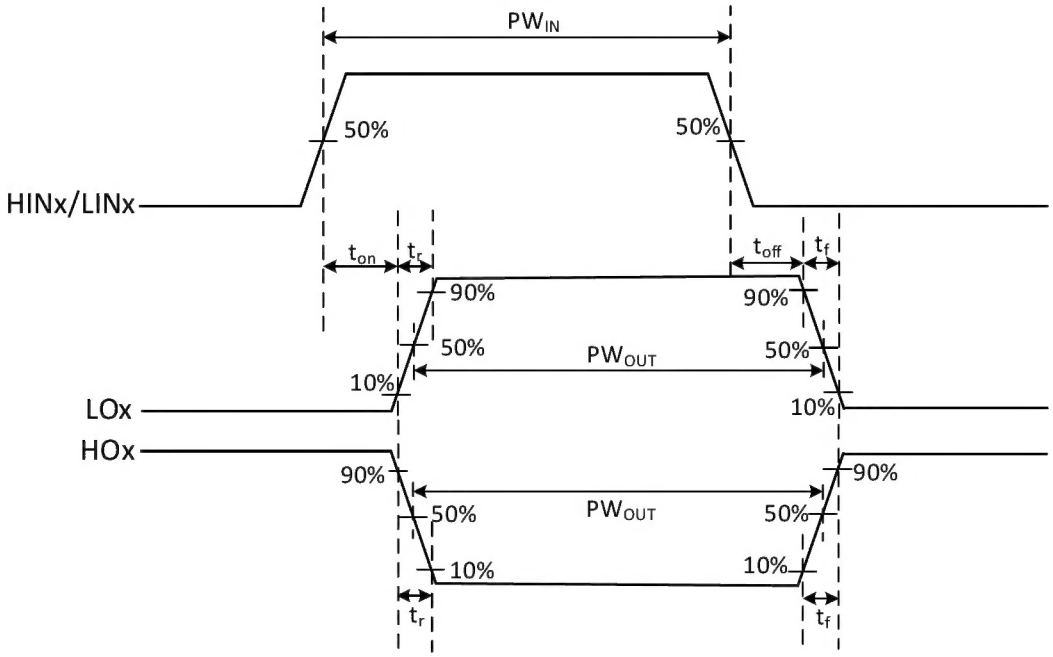
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OHL}	LO high level output voltage	I_{SOURCE} = 20mA	10	11.2	14	V
V_{OHH}	HO high level output voltage (relative to V_{HV})	I_{SOURCE} = 20mA		-170	-280	mV
V_{OLL}	LO low level output voltage	I_{SINK} = 20mA		105	180	mV
V_{OLH}	HO low level output voltage (relative to V_{HV})	I_{SINK} = 20mA	-14	-11.2	-10	V
I_{OH}	Short-circuit pulse current when LO drives high level (used to turn on N-type power tube)	V_{HV} = 15V	100	140		mA
		V_{HV} = 7V	80	115		mA
	Short-circuit pulse current when HO drives high level (used to quickly shut down P-type power tube)	V_{HV} = 15V	500	720		mA
		V_{HV} = 7V	160	230		mA
I_{OL}	Short-circuit pulse current when LO is driven low (used to quickly shut down the N-type power tube)	V_{HV} = 15V	420	600		mA
		V_{HV} = 7V	140	200		mA
	Short-circuit pulse current when HO drives low level (used to turn on P-type power tube)	V_{HV} = 15V	105	150		mA
		V_{HV} = 7V	85	120		mA

6.3.5 Timing Parameters

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	LO output rising edge transmission delay	C_L = 1nF		30	80	ns
	HO output rising edge transmission delay	C_L = 1nF		20	70	ns
t_{off}	LO output falling edge transmission delay	C_L = 1nF		20	70	ns
	HO output falling edge transmission delay	C_L = 1nF		30	80	ns
t_r	LO output rising edge time	C_L = 1nF		75	150	ns
	HO output rising edge time	C_L = 1nF		20	50	ns
t_f	LO output falling edge time	C_L = 1nF		20	50	ns
	HO output falling edge time	C_L = 1nF		75	150	ns
MT	High-side and low-side delay matching			10	50	ns

DT	Dead time		60	90	150	ns
F_{PWM}	PWM switching frequency		0	20	500	kHz

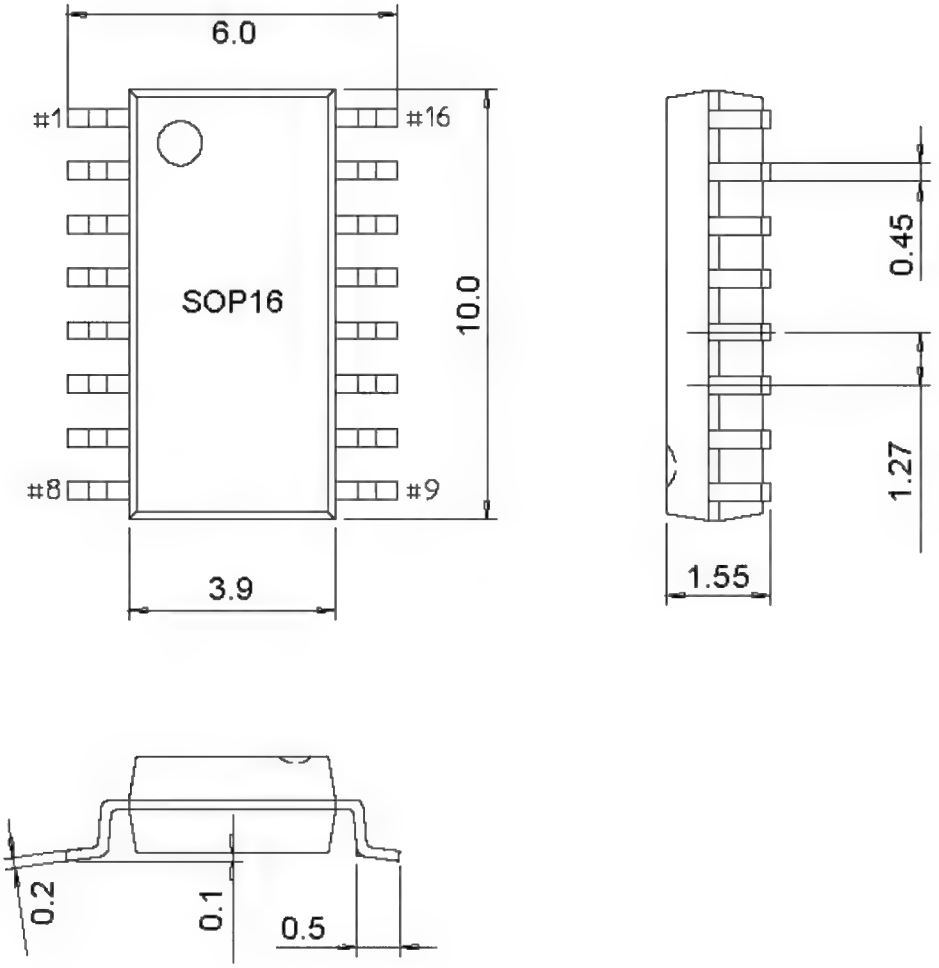
Figure 6-1 Switching timing waveforms



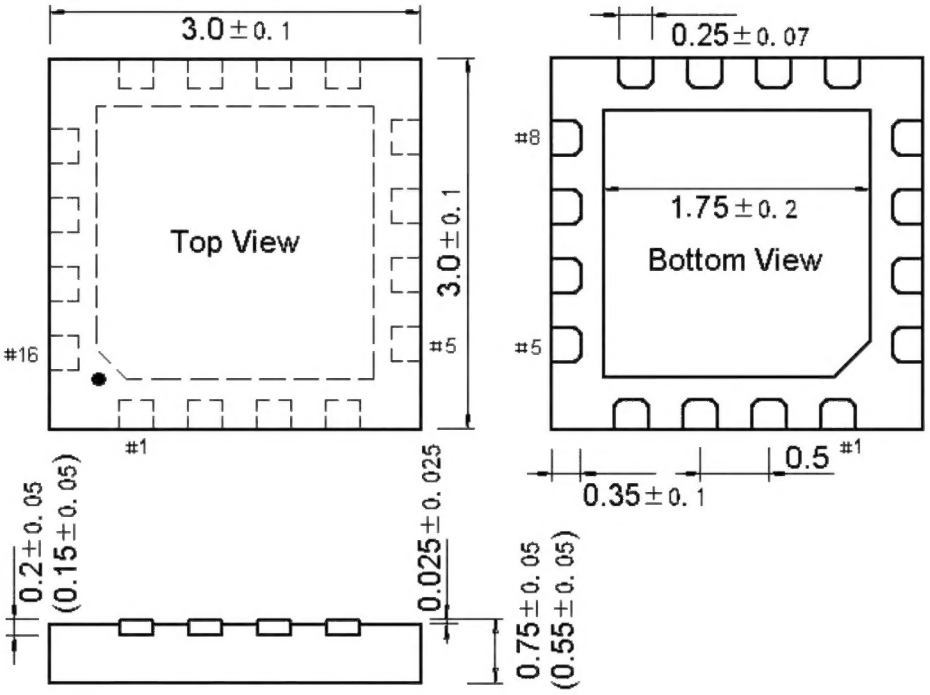
7. Package Information

The dimensioning unit is mm. The pin center distance is a nominal value, the QFN error is not more than ±0.1, and other errors are not more than ±0.2.

7.1 SOP16



7.2 QFN16


3.0±0.1
Top View
3.0±0.1
#16
#5
#1
0.25±0.07
#8
1.75±0.2
Bottom View
#5
0.5
#1
0.35±0.1
0.2±0.05
(0.15±0.05)
0.025±0.025
0.75±0.05
(0.55±0.05)

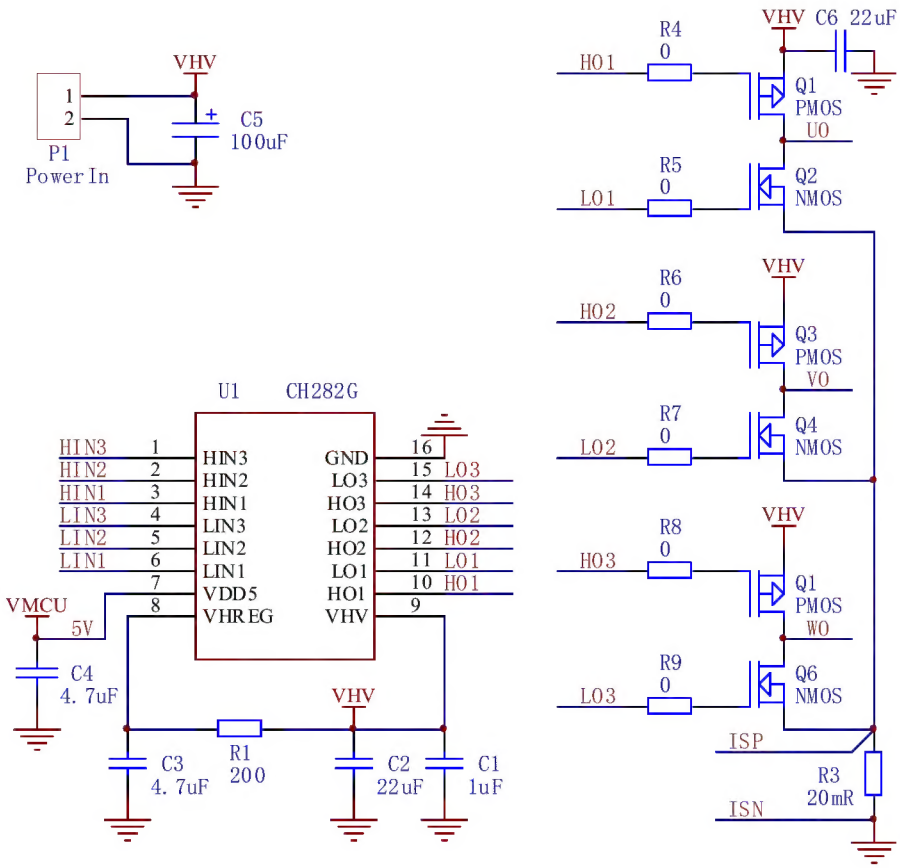
8. Applications

8.1 3-phase N+P Gate Drive

The following figure shows the driving circuit of 3-phase brushless DC motor. LIN1/2/3 and HIN1/2/3 are driven by PWM from controllers such as MCU, Q2/Q4/Q6 are N-type MOSFET power tubes, and Q1/Q3/Q5 are P-type MOSFET power tubes. R3 is the total current sampling resistance, and ISP and ISN provide differential voltage for MCU to amplify and process. R4/R5/R6/R7/R8/R9 are selected according to MOSFET characteristics and EMI requirements.

VMCU is used to provide a simple 5V power supply for MCU, and the optional voltage divider R1 is used to share the power consumption of CH282. Low-power MCU and low-frequency driving applications can short-circuit R1 and remove C3.

CH282P provides PU5L3 pin, and PU5L3 is connected to GND, so VMCU can be selected to output 3.3V voltage.



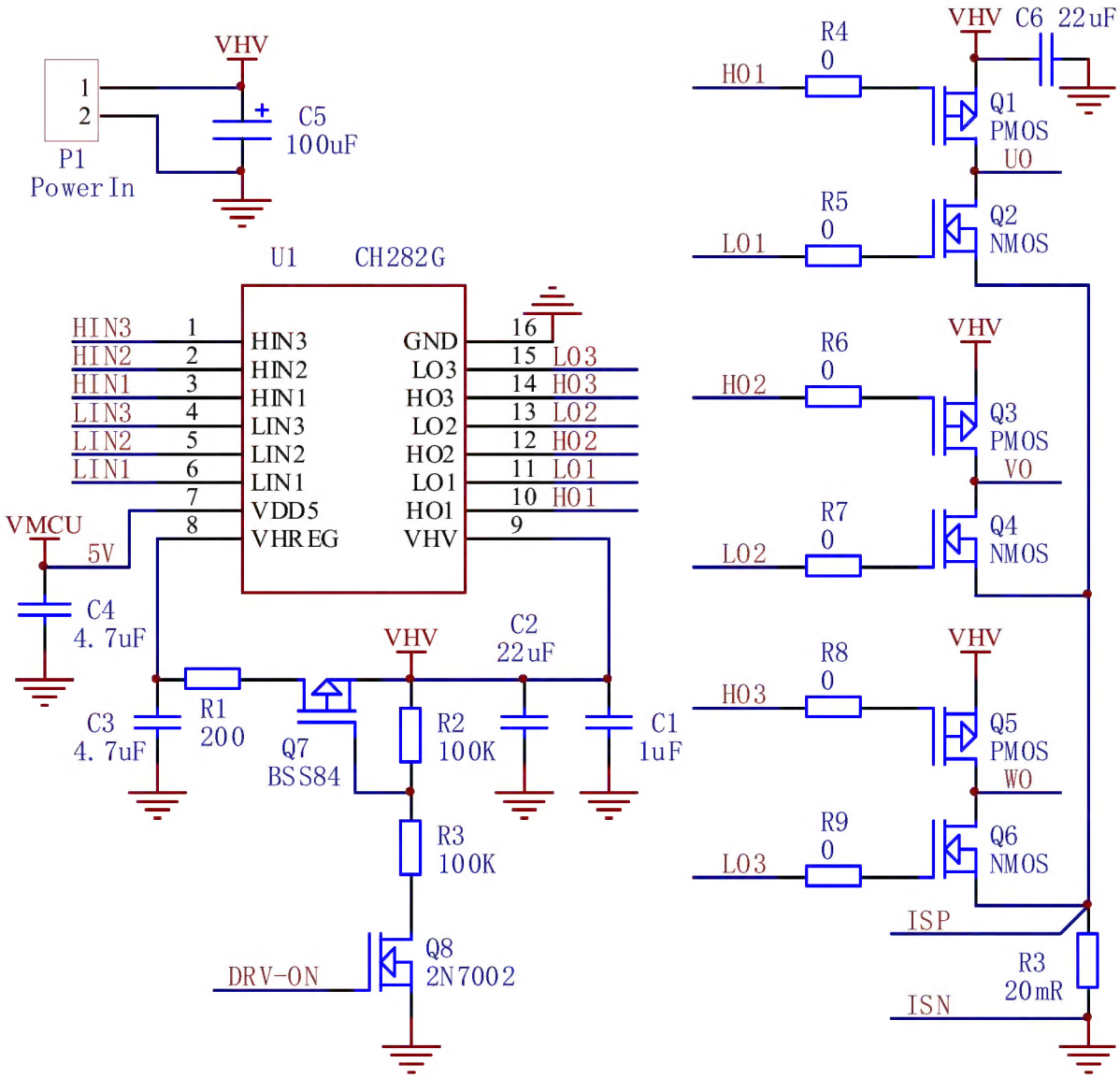
8.2 Ultra-low power Gate Driver in Idle State

When the supply voltage is below 11V, the CH282 idle state all static power consumption is about 50uA, the CH282 can provide power for the MCU, and the MCU sleep can realize the overall low power consumption of about 50uA. If the supply voltage is 20V, then the overall power consumption after MCU sleep is about 120uA.

If further reduction in power consumption at idle is required, then the power supply to the VHREG pin can be disconnected, CH282 enters a reset state, and the VHV pin maintains power supply but draws essentially no current. With this low-power consumption, VHV must be maintained for ensuring that the P-type MOSFET power tubes are turned off; directly disconnecting the VHV supply may cause the P-tube to be turned on, even if a pull resistor is added outside the gate of the P-tube, creating a back-feed of power from the HO pin to the VHV pin.

The following figure shows the circuit that can realize ultra-low power consumption when the gate driver is idle, the MCU is supplied with an independent power supply from another ultra-low power LDO, and resistor R3 is used for voltage divider to prevent the Q7 gate source voltage from being too large, which can be removed when the supply voltage is below 15V.

In the gate drive operating state, the MCU outputs DRV-ON high to turn on Q8 and Q7, and CH282 works normally. In the idle state, MCU output DRV-ON low level off Q8 and Q7, CH282 lost VHREG power supply, enter the reset state, VHV consumption current is close to 0, the whole machine current is MCU sleep current, can be controlled within 5uA.


VHV
1
2
P1
Power In
C5
100uF
U1 CH282G
HIN3 1
HIN2 2
HIN1 3
LIN3 4
LIN2 5
LIN1 6
7
8
HIN3
HIN2
HIN1
LIN3
LIN2
LIN1
VDD5
VHREG
GND
LO3
HO3
LO2
HO2
LO1
HO1
VHV
16
15 LO3
14 HO3
13 LO2
12 HO2
11 LO1
10 HO1
9
VMCU
5V
C4
4.7uF
C3
4.7uF
R1
200
Q7
BSS84
VHV
C2
22uF
R2
100K
R3
100K
C1
1uF
Q8
2N7002
DRV-ON
HO1
R4
0
Q1
PMOS
UO
VHV C6 22uF
LO1
R5
0
Q2
NMOS
HO2
R6
0
VHV
Q3
PMOS
VO
LO2
R7
0
Q4
NMOS
HO3
R8
0
VHV
Q5
PMOS
WO
LO3
R9
0
Q6
NMOS
ISP
ISN
R3
20mR